11/353662

DP ?

WHAT IS CLAIMED IS:

1. A method of testing a device under test, which is adapted to transmit a digital data signal and a clock signal, the data signal being related to the clock signal, to a test device, comprising the steps of:

- sampling within one clock cycle of a local clock signal the data signal and the clock signal by applying a number of strobes for obtaining a corresponding number of bit values each for the data signal and for the clock signal, the strobes having different phase offsets with respect to the local clock signal,

- deriving first comparison results for the sampled bit values of the data signal by comparing the sampled bit values of the data signal each with an expected data bit value according to expected data,

- deriving second comparison results for the sampled bit values of the clock signal by comparing the sampled bit values of the clock signal each with an expected clock bit value,

- deriving combined comparison results by applying logical operations each on pairs of corresponding first comparison result and second comparison result, and

- deriving a test result for the data of said clock cycle based on the combined comparison results.

2. The method of claim 1, wherein the logical operation is one of a Boolean OR operation and an Exclusive OR operation and the step of deriving the test result comprises one of:

(a) checking, whether for each clock cycle there exists at least one strobe, which yields a combined pass result or

(b) checking, whether for each clock cycle there exist only strobes, which yield a combined pass result.

3. The method of claim 1, wherein the device under test is accepted or rejected in response to test results of a plurality of clock cycles of the test device clock.

4. The method of claim 1, wherein the clock signal and the data signal are sampled sequentially with respect to each strobe.

5. The method of claim 1, wherein

- the test device comprises a plurality of data pins, which provide each a data signal and an associated clock pin providing said clock signal,

- performing the logical operation to combine each of the first comparison result with the corresponding second comparison result to determine corresponding combined comparison results, and

- deriving a test result for each of the data of said clock cycle based on each of the combined comparison results.

6. The method of claim 1, wherein the test device first inputs a stimulus signal comprising data and/or instructions into the device under test, such that said device under test generates the data signal and the clock signal in response to said input stimulus signal.

7. The method of claim 1, wherein a clock signal is transmitted by a source synchronous interface of the device under test, such that said clock signal shows transition edges with a constant phase offset with respect to transition edges of its associated data signal transition edges.

8. The method of claim 7, wherein the data signal is sampled according to first strobes and the clock signal is sampled according to second

strobes, both strobe sets or offset to each other by a defined phase value.

9. The method of claims 1, wherein a pass result of the comparison results is represented by a logical "0", and a fail result is represented by a logical "1", and the logical operation, which is applied for receiving the combined comparison result is one of: a logical OR or a logical NOR or a logical "exclusive OR" (EXOR) operation.

10. The method of claim 9, wherein the step of deriving combined comparison results further comprises:

- performing a second logical operation on the plurality of combined comparison results, which refer to different strobes, in order to obtain the test result for the clock cycle.

11. The method of claim 10, further comprising:

- calculating one final accept or reject decision for the device by performing a third logical operation on the test results of a plurality of clock cycles.

12. The method of claim 11, comprising the further steps of:

- determining cycles of the data signal, where no transition of the bit information with respect to an adjacent previous cycle occurs, and

- masking any comparison result obtained with respect to the determined cycles prior to performing the second or third logical operation.

13. The method of claim 1 wherein the strobes are equally spaced with respect to their phase offset with respect to the clock signal of the test device.

14. A software program or product, preferably stored on a data carrier, for controlling the executing the method of claim 1, when run on a data processing system of the test device.

15. A test device testing a device under test, which is adapted to transmit a digital data signal and a clock signal, the data signal being related to the clock signal comprising:

- a sampler sampling within one clock cycle of a clock signal of a local clock the data signal and the clock signal by applying a number of strobes for obtaining a corresponding number of bit values each for the data signal and for the clock signal, each of the strobes having a different phase offset with respect to the clock signal,

- a comparator deriving first comparison results for the sampled bit values of the data signal by comparing the sampled bit values of the data signal each with an expected data bit value according to expected data, and deriving second comparison results for the sampled bit values of the clock signal by comparing the sampled bit values of the clock signal each with an expected clock bit value,

- a processor deriving combined comparison results by applying logical operations each on pairs of corresponding first comparison result and second comparison result, and for deriving a test result for the data of said clock cycle based on the combined comparison results.